NOTRE DAME UNIVERSITY BANGLADESH

VLSI Design Lab Report-01

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Course Title: VLSI Design Lab
Experiment Name: Setting Up DSCH2 & build logic gates

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1 Introduction

The objective of this experiment was to gain familiarity with the schematic-based Electronic Design Automation (EDA) tool DSCH2 and to design, simulate, and verify basic logic gates using CMOS logic. The lab focuses on the schematic representation of fundamental logic gates such as AND, OR, NOT, NAND, NOR, XOR and the functional verification using simulation. The schematic editor DSCH2 was used to create the gate designs and simulate their logical behavior.

2 Logic Gate design in DSCH2

2.1 Inverter / NOT Gate

A NOT gate, also known as an inverter, produces the complement of its input.

Schematic Image

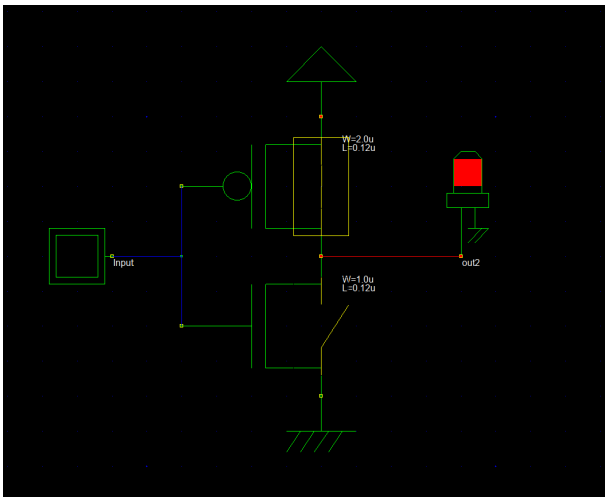

Figure 1: Schematic of the 1-input Inverter

Truth Table

A	Y
0	1
1	0

Observation

From the truth table and simulation results, it is observed that the output of the inverter is always the logical complement of the input. When the input $A = 0$, the output Y becomes logic HIGH (1), and when the input $A = 1$, the output Y becomes logic LOW (0). This confirms that the inverter correctly performs logical inversion for all possible input conditions.

2.2 2-input NAND

A 2-input NAND gate is a universal logic gate that produces a logic LOW output only when both inputs are logic HIGH. For all other input combinations, the output remains logic HIGH. Due to its universality, complex digital circuits can be implemented using only NAND gates.

Schematic Image

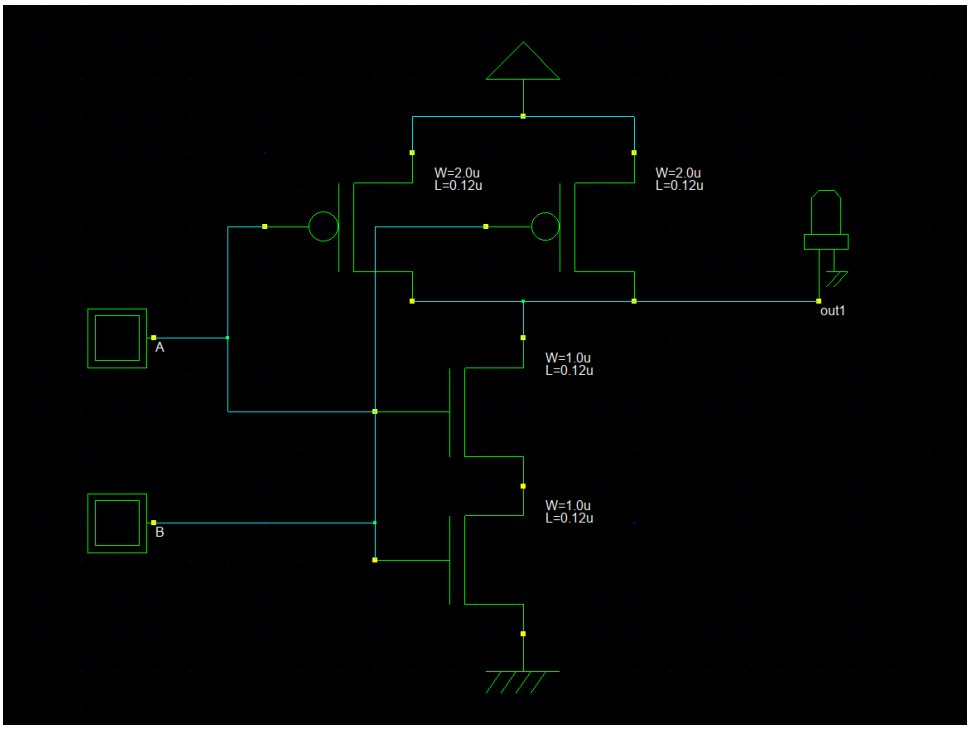

Figure 2: Schematic of the 2-input NAND

Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Observation

From the simulation results in DSCH2, it was observed that the output of the 2-input NAND gate remains at logic HIGH for all input combinations except when both inputs A and B are logic HIGH. When either input is logic LOW, the output stays HIGH. The output transitions to logic LOW only for the input condition A = 1 and B = 1. These observations are fully consistent with the theoretical truth table of a 2-input NAND gate, confirming correct logical operation of the designed schematic.

2.3 3-input NAND

A 3-input NAND gate outputs a logic LOW only when all three inputs are logic HIGH. For any other input combination, the output remains logic HIGH.

Schematic Image

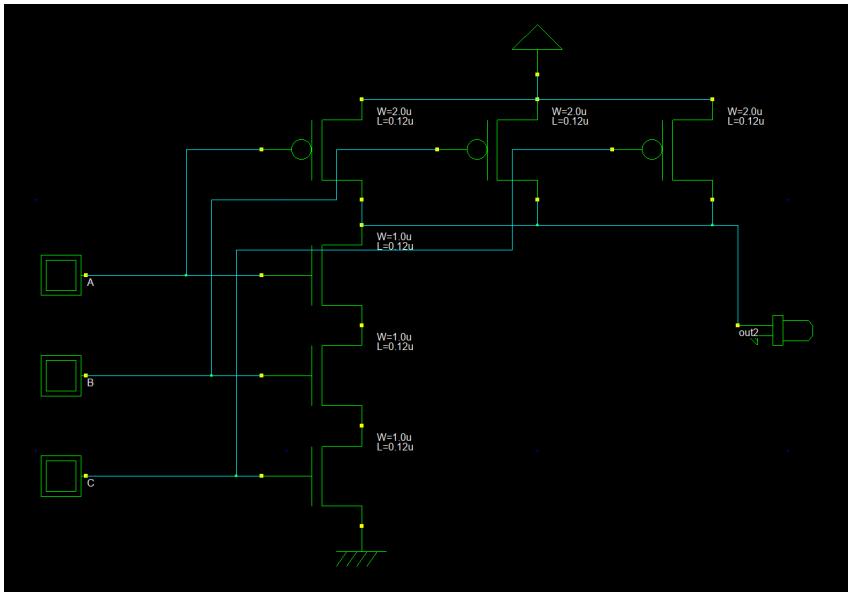

Figure 3: Schematic of the 3-input NAND

Truth Table

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Observation

From the truth table and simulation results, it was observed that the output of the 3-input NAND gate remains at logic HIGH for all input combinations except when all three inputs (A, B, and C) are simultaneously at logic HIGH. In the case where A = 1, B = 1, and C = 1, the output transitions to logic LOW. This behavior confirms that the gate performs the logical negation of the AND operation for three inputs. The observed output values from the DSCH2 simulation precisely matched the theoretical truth table, indicating correct functionality of the 3-input NAND gate.

2.4 2-input NOR

A 2-input NOR gate produces a logic HIGH output only when both inputs are logic LOW. For all other input combinations, the output is logic LOW. NOR gates are also universal gates in digital logic design.

Schematic Image

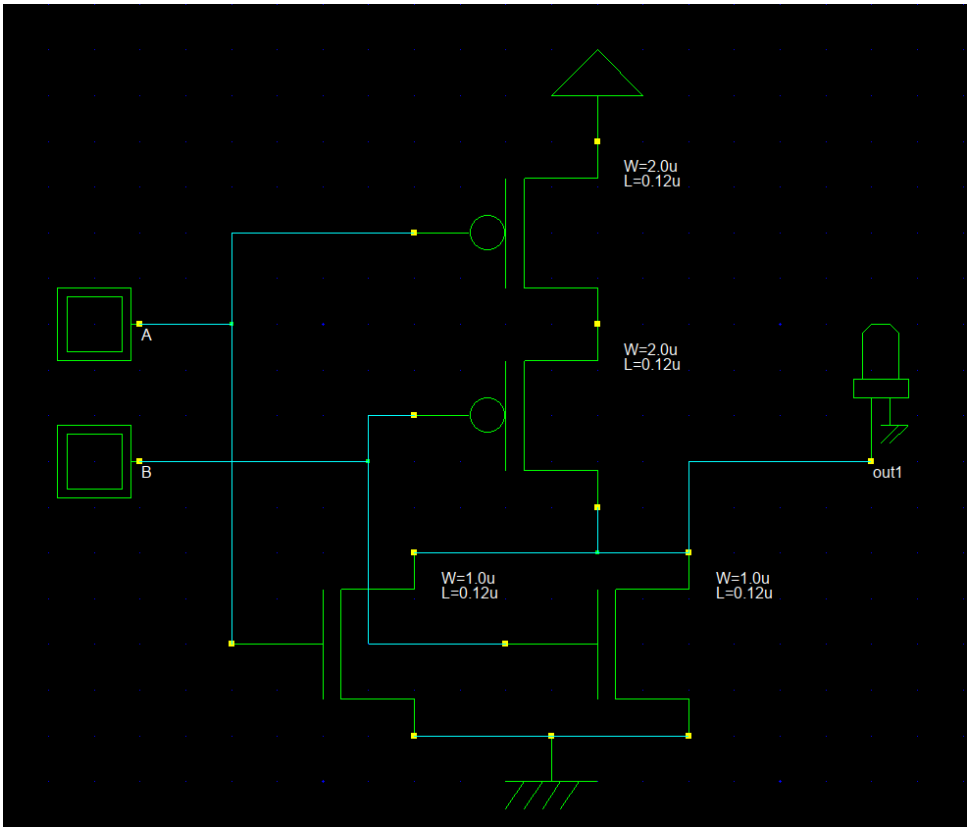

Figure 4: Schematic of the 2-input NOR

Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Observation

From the truth table and simulation results, it is observed that the output of the 2-input NOR gate remains at logic HIGH only when both inputs A and B are at logic LOW. For all other input combinations where at least one input is logic HIGH, the output transitions to logic LOW. This behavior confirms that the circuit performs the logical NOR operation correctly, as verified through DSCH2 simulation.

2.5 3-input NOR

Schematic Image

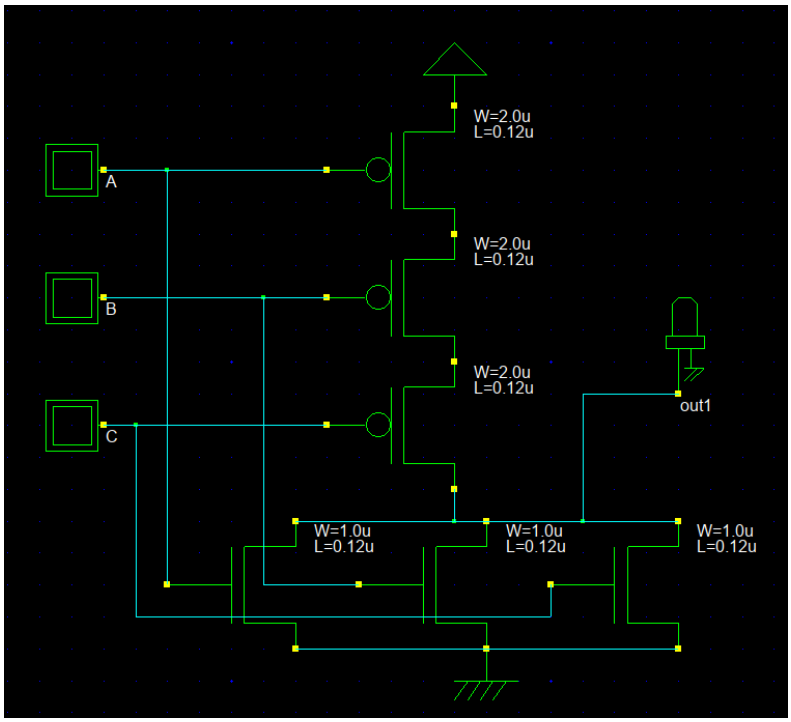

Figure 5: Schematic of the 3-input NOR

Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Observation

From the simulation results, it is observed that the output of the 3-input NOR gate becomes logic HIGH only when all three inputs (A, B, and C) are at logic LOW. For any input combination where at least one input is HIGH, the output remains logic LOW. This behavior is consistent with the truth table of the 3-input NOR gate. The DSCH2 simulation output accurately reflects the expected NOR operation, confirming the correctness of the schematic design.

2.6 AND Gate

An AND gate outputs logic HIGH only when all inputs are HIGH.

Schematic Image

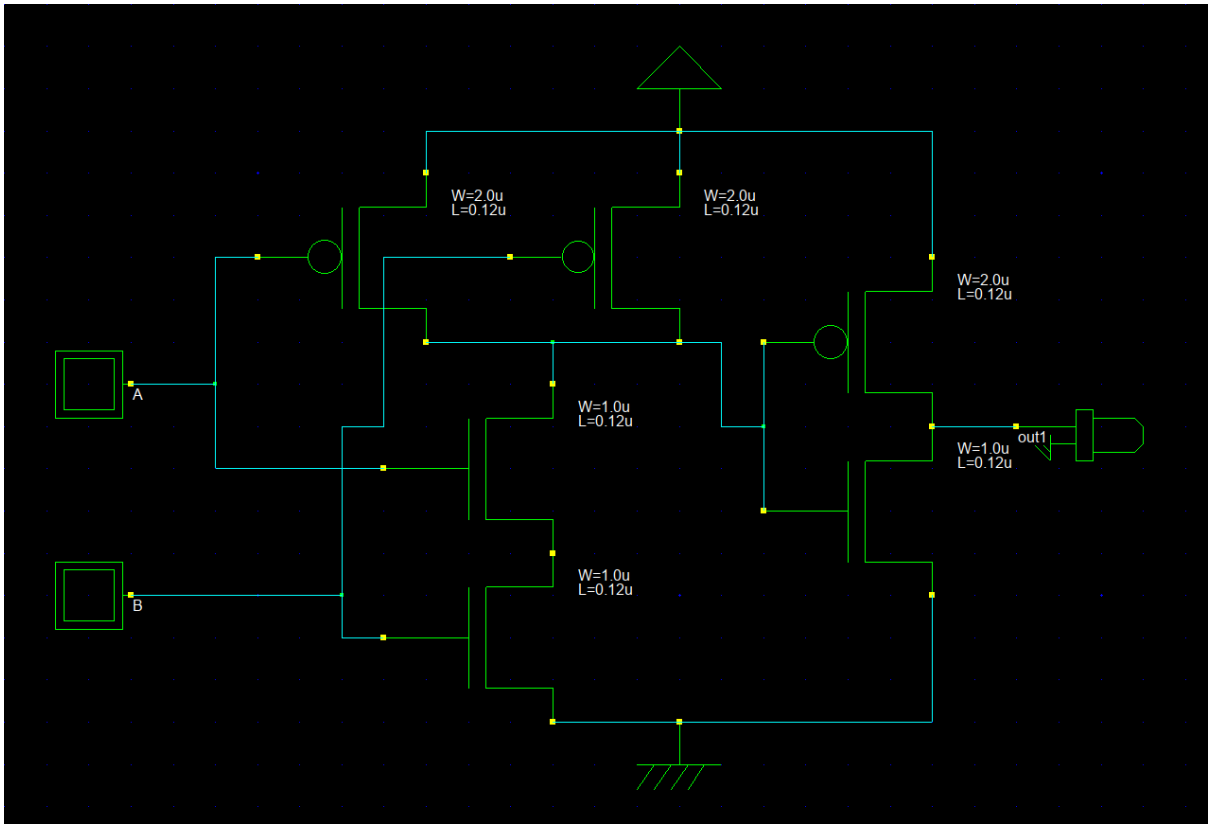

Figure 6: Schematic of the AND Gate

Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Observation

From the simulation results of the 2-input AND gate in DSCH2, it was observed that the output remains at logic LOW when any one or both of the inputs are at logic LOW. The output transitions to logic HIGH only when both inputs A and B are simultaneously at logic HIGH. This behavior is consistent with the truth table of an AND gate, confirming that the implemented schematic operates correctly.

2.7 OR Gate

An OR gate produces logic HIGH when at least one input is HIGH.

Schematic Image

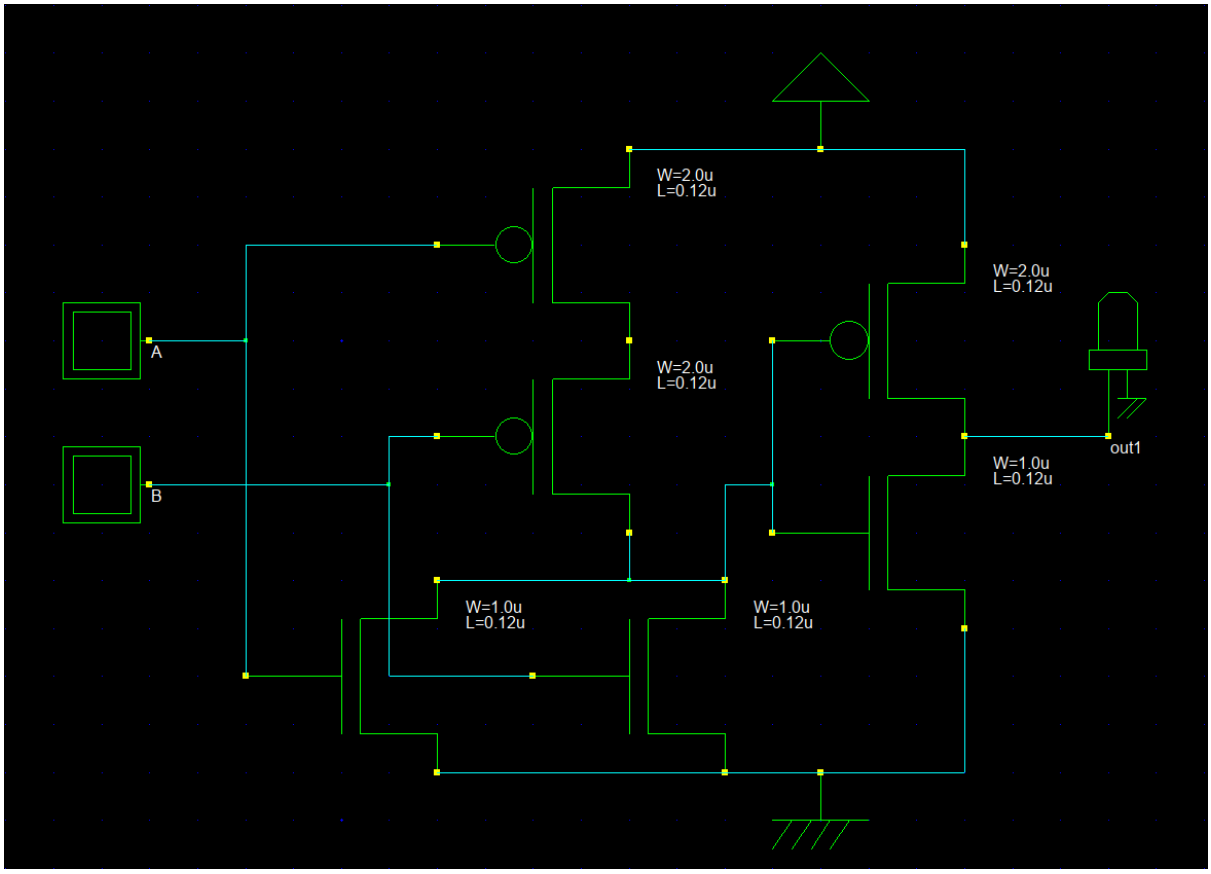

Figure 7: Schematic of the OR Gate

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Observation

From the simulation results obtained in DSCH2, it was observed that the output of the 2-input OR gate becomes logic HIGH whenever at least one of the inputs is at logic HIGH. When both inputs A and B are at logic LOW, the output remains logic LOW. The simulation output exactly follows the theoretical truth table of the OR gate, confirming that the gate correctly performs the logical OR operation.

2.8 XOR Gate

An XOR gate outputs logic HIGH when the inputs are different.

Schematic Image

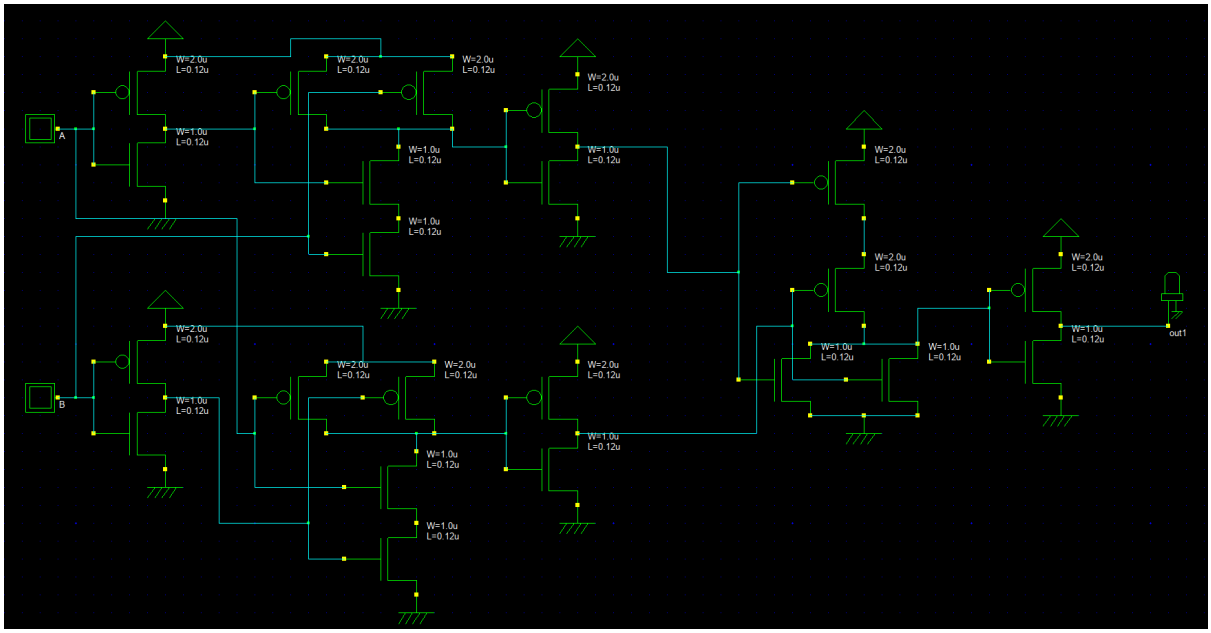

Figure 8: Schematic of the XOR Gate

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Observation

From the simulation results of the 2-input XOR gate in DSCH2, it was observed that the output remains logic LOW when both inputs are at the same logic level, i.e., when both inputs are LOW (0,0) or both inputs are HIGH (1,1). The output becomes logic HIGH when the inputs are different, i.e., for input combinations (0,1) and (1,0). These observations exactly match the theoretical truth table of the XOR gate, confirming that the circuit correctly performs the exclusive-OR operation.

3 Conclusion

In this laboratory exercise, schematic implementations of fundamental logic gates were created and simulated using the DSCH2 environment. For each gate, the simulated out-

puts matched the theoretical expectations based on Boolean logic. This laboratory reinforced the fundamental concepts of digital logic design and the practical use of DSCH2 for schematic entry and simulation.